Chip Reliability

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The major attributes of a semiconductor chip are reliability, cost, speed, and power. While in DRAM the focus is on density/cost and low cell leakage, attention in logic design focuses on speed. Low-power is particularly important in portable electronics and where chip cooling is limited. In all products, however, the main concern of chip manufacturers and customers is on reliability. Throughout the design and development stages of a product, trade-offs are sought between intricately conflicting requirements. For example, there is a trade-off between performance and reliability. The MOSFET hot-carrier reliability is improved by reducing the field near the drain boundary. This can be done by decreasing the drain voltage, reducing the channel length, or implementing lightly doped drain (and source) extensions. All these guards, however, degrade the MOSFET performance. Similarly, reducing the field in the gate oxide improves its reliability, but degrades the MOSFET current carrying capability. A thorough understanding of device failure mechanisms allows optimizing device design and manufacturing processes to simultaneously meet circuit performance goals and reliability objectives. This course presents an overview of important chip failure mechanisms and methods to reduce their impact on chip reliability.

The course is organized in four sessions. The first session describes important silicon devices, technology trends, and basic reliability concepts. Session 2 covers electrostatic discharge (ESD), protection against ESD, and electro/stress migration in multilevel metallization. Single event upsets and dielectric reliability issues are discussed in session 3. Finally, session 4 discusses hot-carrier reliability, latch-up and burn-in. The following is a brief description of the visuals, numbered by session/page.

to ensure that the device itself does not fail and does not substantially degrade circuit performance. Multiple well contacts are designed to avoid latch-up of the structure at maximum operating currents and voltages. Guard rings are placed around the structure to protect against latch-up of adjacent circuits.

2/8-2/12: The three most common ESD models are the human-body model (HBM), the machine model (MM), and the charged device model (CDM). HBM simulates the human body (average capacitance 100 pF, average resistance 1.5 kOhm) MM simulates a machine (tool) that can be charged and then discharged through a component upon contact. The event is more serious than with HBM because of the small discharge resistance and larger capacitance. CDM simulates a die whose components (such as wiring) have been slowly or rapidly charged or discharged. Typically, it is the rapid event that causes most of the damage. Standardized tests are described for the three models.

2/13-2/16: An aluminum or copper base metallurgy is used for global interconnects.There is an increased interest in copper because of its higher conductivity and immunity to electromigration than aluminum. Refractory metals and silicides are used for short local interconnects, layered metallization, and barriers/liners. Patterning of sub-quarter micron dimensions requires planarization because of issues with depth of focus and etching of high aspect ratio features. The dual damascene process is an example of a planarized MLM process.

REFERENCES

[1] T. C. Chen, et al., IEEE Trans. Electron. Dev. 38(4) 941 (1991).
[2] L. Nesbit et al., 1993 IEDM Techn. Digest, p. 627 (1993).
[3] W. Watanabe et al., 1992 IEDM Techn. Digest., p. 259 (1992).
[4] A. G. Sabnis, VLSI Reliability, in VLSI Electronics Microstructure Science, Academic Press, 1990.
[5] D. G. Pierce, IRPS Tutorial 1995.
[6] V. P. Gross, et al., 46th Electronic Comp. and Techn. Conf., May 28-31, 1996.
[7] J. G. Ryan, et al, IBM J. Res. Dev. 39 (4) 371 (1995).
[8] J. McPherson, IRPS Tutorial 1990.
[9] D. Bouldin, IRPS Tutorial 1995
[10] C. -K. Hu, et al., J. Appl. Phys. 74, 969 (1993).
[11] H. H. Hoang, et al., 1988 IRPS Techn. Digest, p. 179 (1988).
[12] J. J. Estabil, et al., VLSI Multilevel Interconnect. Conf., Techn. Digest, p. 242 (1991).
[13] T. D. Sullivan, Annu. Rev. Mater. Sci., 26, 333 (1996).
[14] J. G. Ryan, IBM Microelectronics, private communication, 1994.
[15] A. S. Oates, J. Appl. Phys., 79(1), 163 (1996).
[16] T. C. May, IEEE Trans. Hybrids Manuf. Techn., 2, 377 (1979).
[17] T. J. O'Gorman, et al., IBM J. Res. Dev. 40(1), 41 (1996).
[18] G. R. Srinivasan, IBM J. Res. Dev., 40(1), 77 (1996).
[19] J. Stagg, Appl. Phys. Lett., 31(8), 532 (1977).
[20] M. Kuhn et al., J. Electrochem. Soc., 118, 966 (1971).
[21] A. Toriumi, Device Reliability Tutorial, IEDM 1992.
[22] A. Vollersten, et al., IEEE CMTS techn. Digest., p. 75 (1991).
[23] D. Dumin, et al., IEEE Trans. Reliab., 40, 102 (1991).
[24] W. Weber and M. Brox, IRPS Tutorial 1993.
[25] A. Schwerin, et al., IEEE Trans. Electron Dev., ED-34, 2493 (1987).
[26] K. Watson and R. Bolam, IBM Microelectronics, private communication, 1994.
[27] A. Bryant, et al., IEEE Trans. Electron Dev., 39(5), 1208 (1992).
[28] A. Forcier and A. Wager, IBM Microelectronics, private communication, 1996.

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