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MOS Technology Drivers

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The semiconductor industry has entered a new revolution where connectivity, applications, and an overall pervasive market drives the need for increased circuit density, improved performance, and a decrease in power dissipation. These issues are the backbone for some of the latest silicon technology advancements including the integration of stress enabled transistors and advanced silicon on insulator substrates. Future advancements may include multiple gated devices, high k gate oxides, and band-gap tailored devices.

CMOS performance scaling has been traditionally driven through lithographic image size reduction. The industry is shifting towards performance scaling options that are not necessarily driven entirely by feature size. In general, pervasive computing, or computing on a ubiquitous scale moves the industry into low power technology solutions, while the processor side of computing drives the industry to higher frequency and hence high power technology solutions. A power trend, as seen in figure 1, is rapidly approaching thermal cooling limitations of silicon. This spectrum is again reaching a point where power must be managed as was the case when bipolar transistors were widely in use.

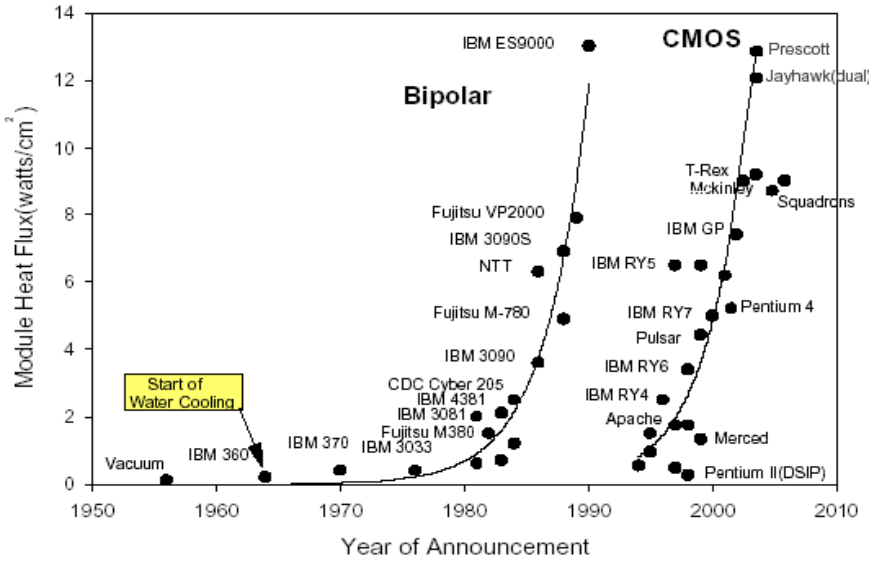

Figure 1: Product power versus performance. CMOS power is now at the level Bipolar power was in the early 90's. Advances are needed to allow for power performance trade-offs.

Clearly the CMOS roadmap if left unchecked will run directly into a power crisis. Innovation beyond simple lithographic scaling must be implemented to balance a power versus performance challenge. This innovation includes novel device structures, new gate electrode and dielectric materials, as well as a means of improving minority carrier mobility. Accompanying this innovation we will again uncover reliability mechanisms both old and new which will require careful analysis and perhaps reliability design rules for mitigation. The industry uses a selected

set of transistor innovations, improvements in the transistor as well as in the metal back end system and in design methodology which are important to consider and implement when optimizing chip power management. Given the tools available now, and those on the horizon, there exists large headroom for reducing the power problem. When does one impose a constraint so that reliability is not compromised? The answer is all the time, considering each technology option, and how a product utilizes each option within its respective design.