This article is part of the IEEE Reliability Society 2008 Annual Technology Report.

Degradation of the high-k dielectric/metal gate stacks under electrical stress

Gennadi Bersuker
SEMATECH
Email: gennadi.bersuker@sematech.org

To sustain the historical rate of transistor scaling, the conventional SiO_2 gate dielectric layer must be replaced with a material that offers a higher dielectric constant *k* (HK). While significant milestones were reached with respect to the performance of high-*k* devices their reliability is still a critical issue which needs to be addressed.

Recent HK reliability studies reflect increasingly complex and diverse gate stack structures fabricated to meet device scaling requirements. Essential progress towards achieving low values of the threshold voltage was made through the introduction of the metal oxide capping layers in gate stacks that, in turn, instigated a number of reliability studies of these systems. Employing fast measurements techniques has provided new insights into the characteristics of the defects in the gate stacks. Interfaces between the high-k dielectrics and high mobility substrates (III-V and Ge), which are being considered for use in transistors in the future technology nodes, have started to attract significant interest from reliability standpoint. In the present study, we focus on the breakdown mechanism of the scaled high-k/metal transistor gate stacks targeting high performance logic applications.

The essential factor, which differentiates HK stacks from the conventional SiO_2 gate dielectric, is that the former is presented by a multi-layer structure, which includes both HK film and thin (usually around 1 nm) SiO_2 layer near the gate stack interface with the substrate, Fig. 1. Such multi-layer structure complicates forecasting reliability behavior in the highly scaled stacks. Indeed, with scaling of the gate stack dimensions, the ratio of the high-k to SiO_2 portions in the total stack thickness changes while each layer is known to exhibit a very distinguish response to the applied electric field. Therefore, lifetime evaluation performed under the accelerated stress conditions on a given gate stack may not be straightforwardly applicable for a scaled down stack. One need to understand which layer contributes the most to the reliability margins in order to focus process improvement efforts on a "weak link" in the gate stack.

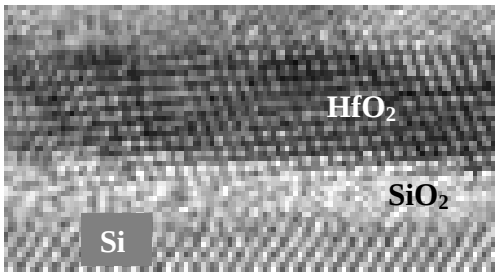

Figure 1. HR-TEM image of the typical gate stack with HfO_2 high-k dielectric and SiO_2 interfacial layer after the standard transistor fabrication processing including the 1000C/10sec source/drain dopant activation anneal

The quality of the interfacial SiO_2 layer in the HK gate stack (hereafter we limit our consideration to the HfO_2 and Hf-silicate HK dielectrics, which are currently used in manufacturing) is known to be strongly affected by processing conditions, which determines to what degree stoichiometry of this layer is affected by its interaction to the overlaying HK/metal films. Indeed, as has been

demonstrated by the electrical, physical (STEM/EELS, ESR, XPS [1-5]) and modeling studies, Hf-based high-*k* films modify the stoichiometry of the underlying SiO_2 layer by rendering it oxygen-deficient. This leads to an increase in its dielectric constant and a higher density of fixed charges in this layer, thereby degrading the mobility of the channel carriers. Precursor defects associated with the oxygen vacancies can be converted to electron traps during device operation under bias, giving rise to stress-induced leakage current (SILC) and contributing to subsequent electrical breakdown.

Previous studies have shown that the evolution of SILC during stress closely correlates to the various stages of the dielectric degradation – soft BD, progressive BD and finally hard BD [6]. This allows employing SILC as a gate stack degradation monitor. Thus, an understanding of the nature and origin of the defects controlling SILC would lead to uncovering of the major contributors to the dielectric BD.

By applying periodically the variable frequency charge pumping measurements (which was shown to probe the electron/hole traps through the thickness of the interfacial SiO_2 film) during the constant voltage stresses at different voltages, we have established a 1:1 correlation between the trap generation and SILC within the wide ranges of the stress times and voltages [7]. This demonstrates that SILC, and hence the stress-induced gate stack degradation is controlled by the

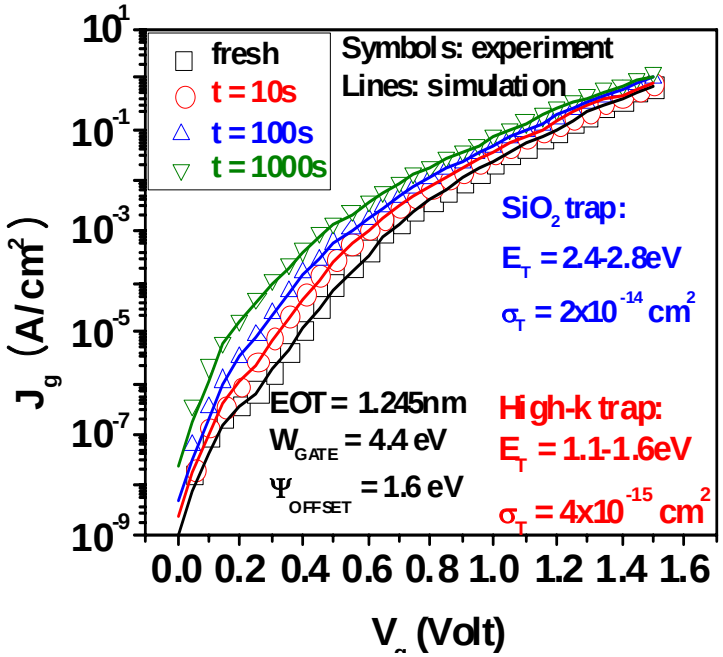

Figure 2. Measured (symbols) and simulated (lines) I_g-V_g curves during 1.1nmSiO_2/3nmHfO_2/TiN NMOS stress at V_g=3V. Information on the energy (E_T) and capture cross-section (σ) values of the stress generated traps in SiO_2 and pre-existing traps in the HK film are included along with the gate stack equivalent oxide thickness (EOT), metal gate workfunction (W_{gate}) and HK band offset (Ψ) values.

defects in the interfacial SiO_2 layer. On the contrary, stress performed on the MIM high-k capacitors (with no interfacial layer) does not show either any trap generation or an appreciable SILC. To confirm the above findings, we performed simulations of the gate leakage current and

SILC during stress using the model, which considers a multi-phonon trap-assisted tunneling conduction mechanism, including random defect generation and barrier deformation induced by the charged traps [8]. An excellent match to the experimental data for both NMOS and PMOS transistors in inversion was obtained (Fig. 2) by using the spatial distribution of stress-generated traps within the interfacial layer as extracted by the above mentioned CP measurements. Electron spin resonance (ESR) measurements performed on the SiO_2/HfO_2 stack of the identical composition and thickness revealed that the generated defects in the SiO_2 layer are indeed the oxygen vacancies with the characteristics g-factor value of 2.0025. Comparison of the temperature dependent time-to-dielectric–breakdown (TDDB) distributions collected on the MIM and MIS structures confirms distinctly different BD origins in the HK dielectric and SiO2/HK stack [7].

Our study demonstrates that the stress-induced defects leading to the gate stack breakdown are generated in the interfacial SiO_2 layer in the HK gate stacks. Control over the SiO_2 layer composition and stoichiometry is critical for meeting reliability requirements for future technology nodes.

References

[1] D. Chi and P.C. McIntyre, APL, 85, 4699 (2004).
[2] G. Bersuker et al, J. Appl. Phys. 100, 094108 (2006).
[3] P. S. Lysaght et al., J. Appl. Phys. 101, 024105 (2007).
[4] J.T. Ryan et al., APL 90, 173513, 2007
[5] C. D. Young et al., TDMR 6, p. 123 (2006).
[6] G. Bersuker et al., IEEE-IRPS, p. 49, 2007
[7] G. Bersuker et al., IEEE-IEDM, p. 791, 2008
[8] L. Larcher, IEEE TED, 50, 1246, 2003