Reliability Society

NEWSLETTER

Vol. 50, No. 4, November 2004

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President's Message

Dear IEEE Reliability Society Members:

As we close out 2004, I am pleased to announce that the Society's ADCOMand EXCOM have begun the difficult but necessary process of re-examiningall aspects of the Society throughout 2004.

Why you ask? Because the Institute is under enormous pressure to changethe manner by which it does business, and that directly impacts everysociety and council under it. For example, if the Institute movestowards an open access policy on scientific publications, then therevenue model that keeps most societies running goes away (and ourSociety and most others rely heavily on the revenue we generate from thepapers we publish). And given that there are other scientificpublishers moving toward the open access model, it pressures theInstitute to move in that direction, and that would directly affect us.

And so given the uncertainty that we are facing, I have challenged ourofficers and elected representatives to look into differing productofferings and revenue models during 2004. And although we have made nodecisions, and await to see which direction the Institute heads in 2005on many important issues, we have worked hard in 2004 to be ready,regardless of which way the Institute heads.

Best Regards,

Jeffrey Voas

mailto:Jeffrey.M.Voas@SAIC.com

From the Editor

Welcome to the first IEEE Reliability Society e-

Newsletter. As in the past with the hardcopy newsletter, an issue will be published quarterly and published to the Reliability Society website.

We welcome your articles, comments or questions. All RS Newsletter inputs should be sent electronically to l.chase@ieee.org.

February	***Inputs due January***
May	***Inputs due April***
August	***Inputs due July***
November	***Inputs due October***

Publishing of advertisements will be available in future issues. Advertisements will be accepted in common graphic format.

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Society Announcements

The RS Officer selections are complete. A complete list of RS Officers for 2005 are:

President -- Jeff Voas

VP Meetings -- Alan Street

VP Membership -- Marsha Abramo

VP Pubs -- Christian Hansen

VP Tech Ops -- Shuichi Fukuda

Secretary -- Bill Tonti (appointment)

Treasurer -- Dick Kowalski (appointment)

Jr PP -- Dennis Hoffman

Sr PP -- Ken LaSala

Pubs appointments:

Way Kuo -- Reliability Transaction Editor

Lon Chase -- Newsletter Editor

The RS Administrative Committee (AdCom) election results are:

Scott Abrams

Shuichi Fukuda

Christian Hansen

Sam Keene

Robert (Bob) Loomis

Ann Miller

Congratulations to the appointees and thank you for your continued contributions to the RS.

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Technical Operations

Society Technical Committee Recruiting Notice

The IEEE Reliability Society national organization is recruiting technical committee members and possibly committee chairpersons for the following technical committees: Software Reliability, System Safety Technology, Human Interface Technology, Mechanical Reliability, Standards & Definitions, CAD/CAE, Microelectronic Technologies, Industrial Systems, Sensor Systems, Information Technology & Communications, Consumer Electronics, International Reliability, Aerospace & Defense Systems, Testing and Screening Technology, Automotive Systems, Energy Systems, 6 Sigma Reliability, Medical Systems, Reliability Design, Warranty, Nuclear Reliability, Maintainability Technology, Assurance Technology, and Emerging (New) Technology.

The basic work for each technical committee consists of developing plans associated with the reliability aspects of the respective field, both present day tactical issues, and long term strategic direction. This is accomplished through four short quarterly written reports that are edited and compiled by the reliability society technical operations editor, and placed in the Reliability Society newsletter, which can be found on our Web site. Additionally, an annual written assessment of the technology in the committee's area of interest is requested. This Annual state of Reliability Technology Report is published world wide, and receives a high level of readership and interest from communities that extend well beyond the IEEE and the Reliability Society. It has become the societies cornerstone publication.

Other work may include the development of standards, guidelines and educational tutorials through the society infrastructure. Working in one of the technical committees is an excellent opportunity to "network" and keep your knowledge current. If you are interested, please contact me and send a short biography with an indication of your experience in the field of interest.

If you do not have a direct interest in either of the above opportunities, please pass this to a fellow reliability, hardware, software, or systems engineering professional who might have an interest.
Thanks for your consideration.

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Reliability and Maintainaibility Symposium (RAMS)

Asian Green Electronics

Nano and Bio Electronics Workshop

Nanoscale Devices and System Integration (NDSI)

International Symposium on Stochastic Models in Reliability, Safety, Security and Logistics (SMRSSL '05)

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JOIN NOW!

Developing Trustworthy Code

Dr. Samuel Keene, FIEEE

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Background

Trustworthy software is reliable, safe, secure, and robust in handling exception conditions. A concerted development focus is required to achieve this quality of software. Quality is the ensemble of all the desirable software attributes. It measures customer satisfaction with the product. Quality is broken down into components that are important to the customer. FURPS is a well-known acronym for software quality. This stands for functionality, usability, reliability, performance, and supportability. Cf. http://www.softwaredioxide.com/ubb/Forum1/HTML/000090.html for a good elaboration of a quality metric suite called FURPS. The reference site breaks these categories down another level of detail. Certainly today, we would add "safe" so the system does no harm, under both normal and aberrant operating conditions. We would also add system security, to mitigate the deleterious effects from a malevolent agent attempts to intrude the system.

Six sigma contribution to product quality

The resultant software product quality is directly proportional to the quality of the software development process that produced it. The six-sigma tool set and process focus helps add better structure and control to the development process. Six Sigma aims to improve both the product as well as its underlying development process. This is one of the hallmarks of Six Sigma. Six-sigma is often thought of as restricted to statistical tools. These tools are a big part of six-sigma but there are other, qualitative tools included in the six- sigma tool suite. This author comes from a reliability background, and chooses to include ALL tools supporting better designs and reliability in the six-sigma schema.

Fundamentally six-sigma is a quantifiable number of field defects to not exceed 3.4 per million opportunities, eg lines of code. Two of the SEI level 5 (top rated) companies have touted to me that they have achieved this level of reliability. One other software company has claimed to better than this level of defects, ie 7-sigma, or higher, reliability. My goal is to quantify the demonstrated level of reliability in terms of its sigma level. For instance, it might be at a 4.5-sigma level and it could be extraordinarily expensive to better that level. It is reasonable to stay at the 4.5 level when cost are excessive to improve the design. This design point decision is being made knowledgably and that is what is desired. The best situation is when the trade off's are fully enumerated and valued in reaching the optimum operating point. The optimum operating point could well be less than six sigma target for a given design.

Six Sigma offers several development initiatives:

- **Requirements management and flow down to lower subsystem levels.** Once requirements are determined, they are flowed down or allocated to the subsystem components. These flow down requirements are matched against the component capabilities to assure the design is capable. There will be trade-offs and iterations here until the design shows it is capable with respect to the stated requirements. Alternative designs can be evaluated using a Pugh matrix or a Kepner-Tregoe decision analysis scheme. Both of these quantitative evaluation tools fit into the six-sigma realm.

  Quality Function Deployment (QFD) can successfully map the design needs (rows of the house of quality) against the engineering solution characteristics (columns of the house of quality). Each column-row intersection is measured in terms of the coupling strength between that engineering attribute and customer requirements. Comments or notes can be inserted into the intersecting cells of the house of quality, where the row or customer requirement meets the developer's solution characteristic. The comments can usefully capture any insights or conditions the development team made when rating the coupling between the design attribute and the customer requirement. So cross-functional teamwork is facilitated using the QFD tool. It also caps the design capability of meeting requirements and stands a monument to the requirements analysis. The maintenance team can review this design analysis to help determine the design impact of any changes.

  Requirements can also be allocated down to lower design levels and checked vs. the component capability to assure adequate margin exists. Sensitivity analysis can assure design robustness under component parameter tolerances.

  Prototypes and iterative designs are the best way to determine and validate system requirements. Requirements are never totally known at the beginning of the development effort. Requirements are rather

an evolutionary discovery effort, on the part of the developer and the customer. This is akin to purchasing a home. The buyer necessarily modifies the home requirements after looking at the home inventory (prototypes). A good requirements process does not end up changing the requirements. It more "discovers" the requirements. Requirements discovery has to be an on-going, aggressive focus for the development team working with the end user

- **Collaborative tools** help promote system and software understanding, eg. Flow diagrams, swim lanes, Pareto charts, cause and effect diagrams. The adage that a picture is worth a 1,000 words applies here. It is easier for a design team to discuss a chart than read the chapter of text needed to explain it. The best development process will enable designers to work in a "caves and common" atmosphere. Collaborative tools are invaluable during design phase. These tools provide "stepping stones" to more understandable, optimized designs. Using an airplane pilot metaphor, the collaborating designers gain a better "situational awareness" of the interfaces and interdependencies. The largest problem with complex systems are getting good requirements and managing system interfaces. Team collaboration tools working in the common area, particularly if the customer is involved, directly address these two system critical areas. Then during implementation, designers will work best in uninterrupted solitude, i.e., working uninterrupted in the "cave".

- **Metrics application and validation**. It is well known that what gets measured, gets improved. So better products will result if the right metrics are measured in a timely fashion. A necessary prerequisite is to assure the measurement system is both repeatable (that any individual can adequately repeat their own measurements) and reproducibility (that other people or test labs can adequately reproduce the original measurements). This measurement validation process is labeled gage R&R. This author believes that most practitioners would be surprised how often their measurement systems are incapable. The gage R&R benchmarks the present measurement capability. Then steps can be taken to improve the measurement accuracy to achieve capable measurements. Variability is the enemy in Six Sigma and gage is the most valuable variability reduction tool.

- **Statistical Decision Support Tools**. My thesis professor once said, "that the hallmark of intelligence is pattern recognition". The automated statistical tools available today help us to routinely extract the signal from the noise. This author help develop the HeNe laser scanners, such as seen in the local super markets. Initially, there was a lot of variation in their observed life under test. Subsequently we found the laser performance variation was driven by the variation in which these lasers were built, even though they were purchased to the same part number. Lab analysis determined they had used different cathode materials (6064 vs 2021 aluminum), different tempers (T4 and T6) and other material variations. All these variations were discussed with the supplier. Eventually a series of designed experiments were run that were designed with the help of the laser manufacturer as well as the user's R&D people. An initial screening experiment was run with 10 input variables at 2-levels and 3 input variables at 3-levels. This was efficiently done with a 32-trial, replicated experiment. More experiments followed. This testing ultimately led to a laser with superior life and performance. This design of experiments (DOE) identified the best materials and design point for the laser. These lasers never were a problem in the scanner application. Also, statistical process control tools (SPC) can be readily applied to detect any product or process changes (so-called special cause variation) vs the common mode variation that typifies the on-going process. So the process can be managed to stay in control.

- **Contingency analysis.** DOE will establish a transfer function relating the output variable (life, power, or noise, in our case) to the critical input variables (cathode material, gas fill pressure, HeNe mix ratio …) The laser performance can be analyzed theoretically or empirically to assure a stable operating point is achieved. It was most desirable that the laser be robust in its performance with respect to nominal variation in its input parameters.

  One of the highest pay-off six sigma tools, this author has found, is Failure Modes and Effects Analysis (FMEA) or its close relative Potential Problem Analysis (PPA). This works best when the reliability analyst meets with the designer and first walks through the design. Then the analyst posits the likely failure modes into each module or component of code. The analyst documents the designer's insight into how the software will deal with that anomalous input. In every instance, this analyst has seen the designer make a change or wish they had thought of this variation before. The FMEA goal is to detect failures when they occur and limit their deleterious impact to the system and the user. The designer is given a copy of the FMEA documenting the diligence of the design effort to produce maintainable and safe code.

Software reliability

Typically software reliability looks at measuring the code reliability or time between failures during the system testing cycle. In this manner software development can be viewed as a "bug removal" process. Test, fix and verify fix. Verification is nominally accomplished by re-testing the code through a standardized set of test cases. This is called regression testing. These testing failures reveal underlying faults in the code. The faults or bugs are then fixed improving the code (unless the fixes added also introduce new defects). The software reliability modeling presumes that the software is running under the proper application "operational profile". So the code "learns" to pass the imposed test conditions. This code refinement anneals the code to the imposed test cases. So the

code's field performance correspondingly improves to the degree that the testing conditions reflect the real world.

John Musa and others pioneered this reliability modeling during software test. There is a convenient suite of these reliability growth models bundled into the CASRE tool suite (Cf: http://www.openchannelfoundation.org/projects/CASRE_3.0/). These tools work best when the code base is stable except for introduced fixes to discovered faults. This is rarely the case. Code maintenance begins as soon as it is written and it nominally continues through out the code's lifetime including the system test phase. There are three predominant types of maintenance:

1. **Perfective changes :** to add functionality to the code.
2. **Adaptive changes:** to accommodate different hardware or interfacing software such as the commercial off the shelf (COTS)
3. **Corrective changes:** to fix bugs

These changes can all add new defects. In fact the most error prone changes turn out to those affecting small number of lines of code. For example, DSC Communications Corp., the Plano Texas Company, signaling systems were at the heart of an unusual cluster of phone outages over a two-month period of time. These disruptions followed a minor software modification. The Wall Street Journal reported, "Three tiny bits of information in a huge program that ran several million lines were set incorrectly, omitting algorithms – computation procedures – that would have stopped the communication system from becoming congested, with messages … Engineers decided that because the change was minor, the massive program would not have to undergo the rigorous 13 week (regression) test that most software is put through before it is shipped to the customer".

Small code changes are not treated with sufficient respect. This story and other infamous software failures can be found at http://mate.dm.uba.ar/~jetchev/Horror/Software%20Horror%20Stories.htm

"Sometimes when I consider what tremendous consequences come from little things …I am tempted to think there are no little things" Bruce Barton

Also we sometimes hear that a bug is discovered that was shipped with original code 5 years ago. The insinuation is that this bug has been latent and escaped detection for all that time period. Typically the situation that triggered and revealed that bug was not in the same code base it was originally released. The code is evolving and the bug could have not been triggered in the initial code release. It could not be reached and activated. The code base is constantly being upgraded and changed. Sometimes deactivated old code, made inactive by a software change, is left in place in safety-critical applications. The maintainers are leery to remove the "dead" or inactive code since they are not totally sure that it might be yet serving some useful function. Or possibly, the dead code will be needed in the future. Every change to the software complicates the code base and degrades the original architecture.

Design for change

Trustworthy code has to be built with code evolution in mind. The software will change and the code documentation and structure must support those changes and give the coder the visibility needed to assure changes goes smoothly. A colleague and myself developed an Excel based system reliability model for the communications system of the new Hong Kong airport. The communications system had many redundancies appropriate for a safety critical system. These were typically k out of n available unit configurations. Then the redundant assets were interconnected to form the Communications system. All the input parameters that were subject to change were put into a separate work sheet and assigned variable names. The model, which was detailed on subsequent worksheets, called for these variable values. The threading of the new variable values throughout the model was automatic. It was easy and secure to change or update any input variables or limiting constraints. This format also made the model variables and constraints obvious to the maintainers. The code reliability during maintenance is directly a function of the code understandability.

Design visibility

Most system and software vulnerabilities result from not having completeness of thought and visibility of the system and how it will be used (operational profile) or how it may be misused. First the development team must work with the customer to gain "situational awareness" of how the customer will use the system and to coordinate the design entities to work cohesively together. Then aberrant input possibilities must be identified and defended against or handled properly. Six sigma has tools to foster cross-team understanding and communication. It also has statistical tools to monitor the internal working of the system and potentially detect and report any unusual behaviors.

Prototypes and iterative development are essential practices for a high quality, trustworthy system. This helps to set proper expectations and gives the customer a real sense of development progress. It also allows the customer to discover more of their requirements and constraints.

Lastly, the main line code always works – or would not have been shipped. It is the exception conditions that cause it to fail over. The FMEA activity can assure the code fails in graceful or expected ways. This can later be demonstrated using fault-injection techniques. It takes an ensemble of tools, a systematic development process,

good cross–functional vision, working together to build understandable code base. Then, this code base is validated running nominal cases (regression testing) and the off-nominal cases (FMEA or fault insertion). This concerted process path leads to developing trustworthy code.

Useful Information
Transactions on Reliability
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Chapters, Committees & Officers
Annual Technology Report
Reliability Society Newsletter
RS Blog
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NEW EDITION OF “SOFTWARE RELIABILITY ENGINEERING” OUT

The new edition of “Software Reliability Engineering: More Reliable Software Faster and Cheaper,” now available, focuses on making software practitioners more competitive without working longer. This is a necessity in a world of globalization and outsourcing where professionals want more time for their personal lives.
John D. Musa has written what is essentially a new book. It reflects the latest software reliability engineering (SRE) practice. Reorganized and enlarged 50% to 630 pages, the material was polished by thousands of practitioners in the author’s classes at a wide variety of companies worldwide.
One of the book’s new features is a series of workshops for applying each area that you learn to your project. The frequently asked questions (answered, of course) were doubled to more than 700. All the popular features of the previous edition have been updated and rewritten. These include the step-by-step process summary, the glossary, the background sections, and the exercises. The user manual for the software reliability estimation program CASRE, downloadable at no charge from the Internet, reflects the latest version. The list of published articles by SRE users of their experiences now numbers more than 65. Everything is exhaustively indexed to make the most detailed topic easily accessible to those using it as a deskside reference.

The book separates basic practice from special situations for faster learning. Musa presents the material in a casual, readable style, with mathematics placed in separate background sections. All this was done to make the book especially effective for self learning. It also furnishes everything you need to implement SRE in your organization, even discussing the most effective methods of how to persuade people to adopt the practice.
One of the first Print on Demand (POD) professional books, it is coupled with a web site (http://members.aol.com /JohnDMusa) for browsing and ordering. The web site has a complete detailed Table of Contents and extensive samples from the book that simulate the bookstore browsing experience. POD uses the latest automated technology to custom print each order and ship it anywhere in the world. It is as fast as you can obtain a traditionally published professional book. The cost is similar. POD technology makes it economic to keep the book in print for as long as even a handful of people want it.
Musa is one of the founders of the field of software reliability engineering. He is an IEEE Fellow and is Engineer of the Year in 2004. Listed in Who’s Who in America since 1990, Musa is a prolific researcher, international consultant and teacher, and experienced and practical software developer and manager. ACM Software Engineering Notes noted for the first edition, “The author’s experience in reliability engineering is apparent and his expertise is infused in the text.”
The book, published by AuthorHouse, comes in hard cover and paperback editions. It contains 630 pages, including prefaces and appendices.

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"More reliable software faster and cheaper"
Software Reliability Engineering website:
The essential guide to software reliability
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Dear family and colleagues,

I am very happy to tell you that I will be assigned to the Congressional office described below for the year 2005, beginning in January and lasting until December, on an IEEE Congressional Fellowship. My duties will be varied but, in general, I will be doing research on technical policy issues, writing speeches for my congressman, participating in hearings, interacting with constituents, and acting as the science advisor to the subcommittee.

Senator Akaka's web site is: http://akaka.senate.gov/

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Our Subcommittee is particularly involved in homeland security issues. The current jurisdiction of the Governmental Affairs Committee is indicated below. However, this jurisdiction may change shortly should the Senate approve the recommendation to rename the Governmental Affairs Committee, the Homeland Security Committee.

This committee and the subcommittee, in particular, under the leadership of Senator Daniel K. Akaka (D-HI), have a broad responsibility for national security issues.

Committee on Governmental Affairs
Full Committee and Subcommittee Jurisdictions
for the 108th Congress

Subcommittee on Financial Management, the Budget, and International Security (FMBIS)

1. The effectiveness and efficiency of Federal financial management;
2. Budget and accounting measures, other than appropriations, except as provided in the Congressional Budget Act of 1974;
3. Federal workforce retirement and other employment benefits and matters relating to the Merit System Principles;

4. Census and collection of statistics, including economic and social statistics;
5. Studying the effectiveness of present national security methods and arms proliferation;
6. The organization and management of United States nuclear export policy; and
7. Studying the intergovernmental relationships between the United States and international organizations of which the United States is a member and relations with other oil producing and consuming countries with respect to government involvement in the control and management of energy shortages.

Committee on Governmental Affairs, to which committee shall be referred all proposed legislation, messages, petitions, memorials, and other matters relating to the following subjects:

* Archives of the United States.
* Budget and accounting measures, other than appropriations, except as provided in the Congressional Budget Act of 1974.
* Census and collection of statistics, including economic and social statistics.
* Congressional organization, except for any part of the matter that amends the rules or orders of the Senate.
* Federal Civil Service.
* Government information.
* Intergovernmental relations.
* Municipal affairs of the District of Columbia, except appropriations therefore.
* Organization and management of United States nuclear policy.
* Organization and reorganization of the Executive Branch of the Government.
* Postal Service.
* Status of officers and employees of the United States, including their classification, compensation, and benefits

IRW 2004 Summary

Attached is a review of IRW 2004, held at the Stanford Sierra Camp from 10/18-10/21 2004.
The review is written by the Session Chairs as noted below.

For 2004: General Chair: Alvin Strong IBM
Technical Program Chair: Rolf Vollertsen Infineon

Keynote:

The keynote speaker, Tim Forhan, Sr. VP of Reliability, AMI Semiconductor, spoke very persuasively about the rate at which the world is changing. This change impacts every aspect of our lives including our business world. Mr Forhan did not use these words explicitly, but conceptually, whereas we used live in a linear world and observe change, we now live in a world of change and observe the rate of that change. Put mathematically, we used to live in the linear realm and observe the realm of the first derivative with respect to time, now we live in the realm of the first derivative with respect to time and observe the realm of the second derivative. This new realm has global implications both in scope, in competition, and in quality. It is no wonder that the world is different today and that today's winner can quickly become tomorrow's loser. Quality is more important than ever and it is expected, but yet its true value must be sold to the customer. And how does one put a value on quality in life-critical applications?

Session 1A: Gate Oxide 1
Session Chairs: Bin Wang: Impinj
Rolf Vollertsen: Infineon
There are three papers presented in this session. They cover topics such as charge-to-breakdown (QBD) modeling, gate oxide NBTI, and effect of Deuterium on QBD and HCI. The session highlights with first QBD modeling paper. The details of the three papers are summarized as following:

GO1-1 (STM): A novel hydrogen release model is proposed to explain the well-known QBD power law dependence. According to the model, the dielectric breakdown is described as excitation, breaking of Si-H bonds and then hydrogen atom diffusion and interaction with pre-existing defects. Validity of this model was demonstrated on high-K stack.

GO1-2 (STM): Correlation between interface generation and stress-induced leakage current (SILC) for NBTI stress was demonstrated. Multiple dissociation energies identified for interface generation indicate that disorder-related reaction model explains better the observed phenomena than the reaction-diffusion model.

GO1-3 (Philips): Researchers have been debating whether Deuterium can affect the device QBD and HCI. In this paper, authors have demonstrated that although post meal annealing with Deuterium improves HCI, however, it does not affect QBD. For post oxidation annealing with Deuterium, no change on QBD and HCI was observed. What is common in those papers is the breakage of Si-H hydrogen bonds in the interface. It happens during QBD, NBTI stress. Paper two demonstrates the correlation between SILC and interface state generation. Obviously, paper three does not agree on it by indicating improved interface state but no improvement on QBD for device with post meal annealing.

Session 2A Gate Oxide 2
Session Chairs: Joachim Reiner: EMPA
Sylvie Bruyere STM

IRW 2004, Session GO2, Gate Oxide – SiO2, Summary:

This session presented two device modelling and two process optimisation papers.

GO2-1 (MACRONIX): This paper presented the charge loss kinetics of a 2-bit ONO memory cell transistor. The charge carriers stored in silicon nitride traps are thermally emitted and pass the SiO2 barrier assisted by tunnelling through cycling-stress-induced traps. No extrinsic data have been given.

GO2-2 (AMD): These authors showed the effect of polysilicon doping levels on tunnelling current and inversion-stress TDDB for plasma-nitrided SiO2 gate oxides between 12.8 and 15.8 Å. The data show a significant influence on the gate capacitance, but none on the tunnelling current and TDDB.

GO2-3 (INTEL): In this paper the authors presented a model for the drain voltage dependence of TDDB of a vertical drain high-voltage tolerant n-MOSFET in a 90 nm node CMOS technology, that results in an increased

allowed operation voltage by taking the voltage drop in the depletion region of the extended drain into account.

GO2-4 (NSC): Experiments to optimise buried layer processing showing the trade-off between gate oxide quality and bipolar performance of a combined bipolar-CMOS technology are presented.

Session 3A Gate Oxide 3
Session Chairs: William Knowlton: Boise State
Yuan Chen: JPL

There are four papers presented in this session.

GO3-1: Bin Wang, et al., from Impinj Inc., studied the SILC and charge loss of nonvolatile memory cell by using a floating-gate integrator technique. With capability of resolving currents as low as 3x10-22 A by this technique, the relation between SILC and Vox was established to extrapolate a 10-year retension lifetime of a memory cell with 7nm gate oxide thickness.

GO3-2: Michael Ogas, et al., from Boise State University, investigated the impact of pmosfet stress-induced degradation on inverter circuits. It was observed that stress induced low leakage (Ig-Vg) in 2nm pMOSFETs led to a Vsp change in inverter VTC and considerable change in the time domain which was directly related to significant changes in Vt, Id,sat and Gm,max.

GO3-3: Joachim Reiner, from EMPA, observed pronounced reversible switching behavior in pmosfers with 3.5nm gate oxide when stressed in inversion mode. The cause for this reversible, pre-breakdown leakage current switching phenomenon was proposed to be the trapping and de-trapping of electrons into or out of the positively charged traps within the oxide layers.

GO3-4: Andreas Kerber, et al., from Infineon Technologies, proposed and developed a fast wafer level current measurements (nA to mA) setup using analog input/output PCI card and a (log-lin) current-voltage converter. Verified by TDDB measurements on SiO2 and charge trapping measurements in HfO2, a resolution of 50usec was realized, which is orders of magnitude faster than GPIB-controlled-SMU setup.

Session 1B Interconnects 1
Session Chair: Harry Schafft: NIST
Lynette Westergard: AMI Semiconductor

Session 1B covered the waterfront of the issues related to the thermal and reliability challenges resulting from the introduction and use of low K dielectric materials in a regime of ever greater packing and stacking densities. On the one end, Baozhen Li of IBM, using analytical models, showed how the use of low K materials, with their relatively low thermal conductivities impact safe current-carrying capabilities, electromigration reliability, and design considerations of copper interconnects. On the other end, Alvin Strong, also of IBM, using a finite element method tool, showed the results of heat-flow ramifications for a variety of simple patterns that compared well with the results of physical measurements. In between was the paper by David Ney of STMicroelectronics. Here the message was that accurate knowledge about the thermal conductivities of low K dielectrics is needed for optimal thermal management of present and future ICs. With the use of analytical expressions to analyze the results of joule heating in test lines imbedded in various dielectric configurations, it was shown how the thermal conductivities of low K dielectrics, such as fluorinated silicare glass, phosphorous silicate glass, and silicate carbide oxide could be determined.

Session 2B Interconnects 2
Session Chair: David Catlett:TI

Four papers were presented in this session focusing on the physical dimensions and properties of Cu damascene lines that contribute to stress voiding in circuits.

IC2-1: The first paper from Phillips Semiconductors proposed a kinetic model for stress migration that takes into account interconnect geometry, vacancy diffusion, and temperature extrapolation to model the acceleration of voiding. This paper concluded the width dependence of void formation from the larger vacancy reservoir and potentially larger mechanical stress.

IC2-2: The second paper from STMicroelectronics showed results from tests structures with varying ratios of vias to line length that allowed for the separation of different Cu diffusion paths for narrow versus wide lines. This study concluded lower EM robustness for large lines relative to small lines around operating conditions.
IC2-3: The third paper from Simon Frasier University presented axisymetrc 3- and 2-dimensional numerical models to simulate the instabilities driven by capillary and electron wind forces that lead to specific voiding patterns in Al and Cu lines.

IC2-4: The last paper, from LSI Logic Corporation, discussed results of a model for electromigration induced

voiding in Cu lines that included interface bonding strengths which significantly influences the location of the onset of voiding. Results were compared with in-situ SEM experiments.

Session 3 Interconnects 3
Session Chairs: Krish Mani: CM Innovations
Harry Schafft: NIST

General overview:
In Session 3B, electromigration-related reliability problems were discussed from two distinctly different perspectives. Now that Al is being replaced by Cu, people feel that they can push copper lines more than they could in Al technologies. But, said Martina Hommel of Infineon Technologies, they forget the impact on the Al pads that have to conduct the greater currents. Electromigration robustness of the bond pads now has to play an important role. She showed that the electromigration life time depends on the usable Al reservoir, which depends, in turn, on the pad design and the effective current path. An increased aluminum thickness and an additional second via array improves the pad reliability significantly. Donald Gajewski of Freescale Semiconductor reported that cladding the top of the Cu interconnect results in much better electromigration performance with regards to median time to failure and activation energy. This paper had a focus on MRAM type applications.

IC3-1 " Electro migration-limited lifetime of Aluminum bond pads" Martina Hommel et al
The electro migration (EM) issues with Aluminum (Al) led to the introduction of Copper (Cu) with its significantly higher EM resistance and lower resistivity in to the mainstream Semiconductor processing. During the operation of the Integrated Circuit(IC) all the current to and from the chips interface has to flow thru the Al bond pads. Hence it is vital to analyze the EM resistance of the bond pads under stress conditions.
The current work presented experimental data on different realistic scenarios of the current industry standard metallization schemes with Al bond pads. The results show that the EM resistance of the Al bond pads can be improved by increasing the thickness (a process solution) of Al. The improvement results from reservoir effect. Addition of an extra array of vias (a design solution) also helps reduce the EM degradation of the bond pads. This work also verifies that the measurement method itself did not have influence on the phenomenon being measured.

IC3-2 "Electro migration of MRAM customized Cu interconnects with cladding barriers and top cap" Donald A. Gajewski et al
The EM issue of a promising Non Voltile Memory such as MRAM is of immense importance as it involves forcing significant amount of current thru copper wires during the operation of the product. This work studies the effect of cladding the copper lines on its EM performance. The experimental data shows that the cladding of copper with a soft ferromagnetic material along with Ta diffusion barrier significantly increases the EM performance of copper wires. The cladding cap limits the failure mechanism to grain boundary diffusion and eliminates the surface diffusion path along Copper Nitride interface observed in conventional CMOS processes. The activation energies were found to meet or exceed MRAM product reliability requirements.

Session4 Hot Carriers
Session Chairs: William Tonti IBM
Guoqiao Tao, Philips

Three papers were presented in this session.

HCS-1: The first paper "A Comprehensive Analysis of NFET Degradation due to Off-State Stress is from Infineon Technologies AG, and Nanya Technology Corporation.
Bulk MOS devices were studied in the off state condition, i.e. Drain high, gate-source-and bulk node at ground. The devices used in this investigation were 45ang. I/O devices where a typical LDD was replaced by a high energy and dose implant. (Effectively changing the device design and moving away from the LDD design point). During NMOS stress (85C, Vd =3.5V) Positive charge and electron traps were created at the drain boundary. This is influenced severely by the off current dependence, i.e. the short channel effect. Device degradation followed a slope ~0.5, comparable to DAHC. A V model extrapolation is reasonable for lifetime extrapolations for V > 3.0volts. However for Low V extractions a 1/V model is needed, as the V model tends to be too optimistic in this regime.

HCS-2: The next paper "New insights in Threshold Voltage Shift for UltraThin Gate Oxide" from the University of Maryland and the National Institute of Standards and Technology uses constant voltage stressing (CVS) of PMOS and NMOS devices (Bulk Si, Tox=2nm, Area=50x50μm2). Threshold Voltage, Vt is monitored and the underlying reason for the Vt shift is studied. In general most researchers believe (+) and (-) traps generated at the Si/SiO2 interface are responsible for the VT shift in P and N MOS fet's respectively. Stressing was accomplished using two methods. In the first method the gate is DC stressed relative to all other terminals grounded, and in the second method the gate is stressed at 10Mhz, with the bulk, drain and source at a potential of Vosc=5mV. Thus, Method 1 is a DC stress method(Using an HP 4156), while Method 2 is CV method(Using an HP 4284LCR meter). For NMOS: Vth shifts monotonically increase (becoming more positive)with Qinj independant of stress. For PMOS the Vt shifts are monotonically decreasing (The VT is becoming more negative) independent of stress conditions. Simulation was used to understand the nature of the shifts observed both in N and P MOS were found

to correlate to the measured results by varying the interface scattering density (NSCAT) in the NCSU Mob 2D simulations, as apposed to varying the Coulombic charge density (Qox) at the interface. This is due in part to the inherent reduction in channel mobility which is tied to Nscat. The net is that general notion of Vt shifts being the measurable result of Qox screening requires a deeper investigation. In addition, the CV and DC shifts produced different levels of Vt versus time results indicating that both DC and AC device use should be incorporated when investigating lifetime.

HCS-3: The last paper of the HC session is “Anomalous NMOSFET Hot Carrier Degradation Due to Hole Injection in a DGO CMOS Process”. This paper is presented by the National Semiconductor Corporation. The hot carrier effects of a pre-metal etch stop (SiON) on a 3.3V dual gate oxide I/O device are investigated. The anomalous behavior is observed at ~70K seconds of DC stress where prior to this time device Idsat is decreasing with applied high voltage stress. At this point in time the device partially recovers (i.e. Idsat increases), and post 70K seconds the device degrades at a much higher slope than prior to the anomalous recovery. The SION deposition conditions (SiH4 flow rate) was experimentally determined to directly influence this anomalous behavior. For example, a flow rate = 50 had little to no anomalous behavior, while a flow rate of 100 had a highly unacceptable anomalous behavior.
The abrupt change in Idsat was directly correlated to the measured Vt. It experimentally is shown at 70K seconds the anomalous degradation is consistent with hole (positive charge) injection, while for T> 70K seconds the degradation is consistent with electron injection and subsequent trapping. Idsat was shown to follow the anomalous observation, while Idlin was shown to not be affected, and is more in line with expected systematic Idsat (reduction therein) degradation. Simulation was used to substantiate the device current flow in linear and saturation modes, and substantiate the observations. The conjecture is the Si/SiO2 interface is weakened by higher SiH4 flow rates or that a net hydrogen rich SiON film results in a manner such that positive charge may be trapped in the center of the device a secondary impact ionization site results. Simulation indicates there is a hole current traveling at the Si/SiO2 interface and may be responsible for these hole traps. This results in charge separation and the anomalous Idsat degradation behavior.

Session5 NBTI
Session Chair: Amr Haggag: Freescale

NBTI has emerged as a major reliability concern in leading edge technologies. NBTI causes an increase of Vt and concomitant effect on other device parameters such as Id, gm, etc. Active at low Vg and activated by high temperature, NBTI causes fixed positive charge in the SiO2 and interface states at the SiO2/Si interface. In general, the fixed charge can be removed, while the interface charges cannot, by turning off the channel. NBTI can be strongly aggravated by processing effects such as excess N or B, H2O incorporation, or plasma-process-induced damage, while NBTI can be reduced by modest amounts of F. These effects can also lead to an apparent gate length dependence due to the higher length to area ratio. Time- and voltage-dependent models are still being investigated, since more understanding is needed about the NBTI kinetics (diffusion-limited vs. reaction-limited). Diffusion-limited kinetics help to explain sublinear time-dependence of NBTI but so do reaction-limited kinetics that factor in disorder as shown by Haggag et. al. in 2001.

NBTI-1: This year Vincent Huard et. al (STM and Philips) provided further evidence of the reaction-limited kinetics that factor in disorder and showed NBTI data suggesting the sublinear time-dependence exponent of NBTI is temperature dependent as predicted by this model.

M. Denais et. al. (Crolles Alliance of STMicroelectronics, Phillips and Freescale) provided a model of the oxide field dependence. While some argue power-law and some argue exponential, M. Denais data and model support exponential. They also invoked reaction-limited kinetics with disorder.

NBTI-2: B. Zhu et. al. (NIST) presented a closed form model for NBTI under AC conditions again based on the generation and reduction of the fixed charge created during NBTI.

NBTI-3: J. Campbell et. al. (Penn State , TI) showed atomic measurements of the defects involved in NBTI and measured Pb-like center (interface traps) and E'-like centers (hole traps possibly also the fixed charge in NBTI). NBTI damage also has a strong relaxation effect due to bulk charge de-trapping or some believe interface state re-passivation. It is therefore critical to develop test methodologies that do not unnecessarily underestimate the lifetime projections.

NBTI-4: In the final paper of the session M. Denais el. al (STM , Philips) presented about their novel 'on the fly technique' where measurements of the Id shift are measured without removing the stress voltage. In the evening workshop of NBTI, everyone also noted that the “failure criterion” is also subject to discussion and interpretation: is the criterion 10-30mV, or do customers need to know by how much Vt will shift after 10 years? The definition of “failure” is often circuit- and application-specific, so the appropriate parameters need to be examined.

Session6 HiK
Session Chairs: Chad Young: Sematech
John Conley: Sharp Labs of America

The theme of this year's High-k Session turned out to be the impact of fast transient charging on the evaluation of hafnium-based gate dielectrics. The rapid trapping and detrapping of electrons during substrate injection causes is responsible for a significant portion of Vt instability, impacts mobility extraction, and confounds reliability extrapolation. The talks in this session generated many questions and much discussion.

HIK-1: Some notable results include the conclusion by Ribes, et al., (STM and Philips) based on pulsed I-V techniques, that pre-existing traps sites are located 0.35 eV below the high-k conduction band and have a Poole-Frenkel detrapping mechanism.

HIK-2: R. Choi, et al., (Sematech) suggested that drain to gate stress can damage the area of the high-k gate dielectric near the drain, resulting in asymmetric subthreshold swing degradation.

HIK-3: H. Harris, et al., (Sematech) showed that the subthreshold slope or peak transconductance did not degrade with stress time while a shift in Vt with time was seen, suggesting that fast transient charging, rather than hydrogen release induced interface trap creation, may be the primary source of NBTI.

HIK-4 : J. Sim, et al., (Sematech) stated that both “cold” and “hot” carriers in hot carrier stress (HCS) measurements contribute to the observed Vt shifts, that HCS induces more reversible electron trapping than constant voltage stress, and that TiN gate devices show improved stress stability over poly.

HIK-5: G. Bersuker, et al., (Sematech) in an entertaining talk, provided a mobility extraction technique based on pulsed I-V measurements that corrects for the contribution of fast transient charging on the channel mobility of nMOSFETs.

Respectfully Submitted:
William R. Tonti
IRW 2004 Communications Chair.

Dallas Chapter

By Lon Chase, Chapter Chair

Chapter Programs

The Dallas chapter is continuing its program of technical presentations with the following.

Subject:"Tin Whisker Acceptance Test Requirements"
Date: September 21, 2004
Speakers: Mr. Joe Smetana, Alcatel

Program Summary:
The transition to lead-free has returned an old problem, tin whiskers, to the forefront in electronics assembly. Tin whiskers are a spontaneous columnar or cylindrical filament, which rarely branches, of mono-crystalline tin emanating from the surface of a plating finish. Tin whiskers are a reliability concern. They can cause electrical shorts, disruption of moving parts, and/or degraded RF/High speed performance. In spite of more than five decades of research done on tin whisker growth, a basic understanding of the mechanisms that control whisker growth and prevention remains elusive. Furthermore, both because of this lack of understanding as well as the fact that whisker formation appears to decelerate at temperatures significantly above 60°C, accelerated test conditions and extrapolation models are not yet well established. Pure tin (or other high tin content alloys) are not immune to whisker formation. In spite of the lack of understanding, the industry is moving towards Pb-free electronic devices and assembly. The NEMI Tin Whisker Users Group has developed an acceptance test that is a combination of tin-whisker mitigation practices, process controls and tin whisker testing to reduce the risk problems associated with tin whiskers. This document has been submitted to IPC and to JEDEC to create appropriate industry standards. The presentation will provide an overview of this document and provide the rationale behind the criteria it includes.

About The Speaker:
Joe Smetana is a Principal Engineer, Advanced Technology at Alcatel. He is also a Distinguished Member of the Technical Staff of the Alcatel Technical Academy. He is the technical lead for Alcatel's worldwide lead-free and RoHS activity. Additionally, Joe is chairman of the NEMI Tin Whiskers User Group and is also actively participating in the NEMI Tin Whisker Modeling Project and the NEMI Tin Whisker Accelerated Test Project. Joe also currently chairs the HDPUG (High Density Packaging User Group) Consortium Via Integrity with Lead-Free Processing project and has been very active in various consortium projects involving lead-free assembly and reliability.

Prior to joining Alcatel, Joe served at Texas Instruments as Lead Engineer for Weapons Systems Division Producibility Engineering from 1985 to 1990. He also served as a Nuclear Engineering Officer in the US Navy from 1980 to 1985, primarily working shipyard overhauls of nuclear powered cruisers. He qualified as a

Chief Engineering Officer for Naval Nuclear Power Plants and as a Surface Warfare Officer during this time.

He has a Bachelor of Science degree in Electrical Engineering from Tulane University, as well as graduate studies in Nuclear Engineering with the US Navy. He is a Licensed Professional Engineer in the State of Texas.

Denver Chapter

By Sam Keene, Chapter Chair

Denver Chapter had Prof Chuck Rick make a presentation on left brain problem solving techniques. There were 40 people attending.

The Denver Reliability Chapter supported the Section Conference with three presentations:

1.The Reliability of DC to DC Power Converters: Bill Tian

2. Producing Embedded Flight Software with Agile Commercial and Government Practices: Jon Hagar and Randal Smith

3. Six Sigma Contributions to Reliability: Sam Keene

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Japan Chapter

As I wrote in the August issue of this Newsletter, the Japan Chapter held its annual symposium on risk engineering on October 1 at the Tokyo Campus of the University of Tsukuba. The topic of this year was, “Human-machine collaborations in an emergency.” Toshio Tsukahara (Capt.) and Tetsuaki Nakagawa (First Officer) of the Japan Airlines delivered a remarkable lecture for the topic, based on their experiences and simulation studies.

Firstly, they explained functionalities of various automated warning systems in the flightdeck, such as the stall warning system, the takeoff warning system, the wind shear warning system, the enhanced ground proximity warning system (EGPWS), and the traffic alert and collision avoidance system (TCAS). Secondly, they classified the automated warning systems into some categories from a human factors point of view. Human control behavior can be skill-based, rule-based, or knowledge-based. The automated warning systems can thus be classified by the criterion, “which level of human control behavior the warning system is supposed to support or enhance.” Based on the classification, they extended their discussion how human pilots can collaborate with the automated warning systems in situational recognition, decision-making, and action implementation.

Finally, Capt. Tsukahara and Mr. Nakagawa gave us their research results on pilot procedures (specified by the Operation Manuals) and aircraft performance under the circumstances when TCAS sets off a resolution advisory, such as “Climb, climb, climb!” at very high altitude (say, 32,000 ft). They conducted a field study and simulator investigations with the help of their colleagues. They investigated capability and efficacy of several control strategies for collision avoidance. One of the strategies is the one currently in use, and some of them are brand new.

Airline pilots, aviation researchers, authorities, and reliability and safety engineers/researchers of non-aviation domains, such as automobile, trains, and process plants attended the symposium. The total number of audience was around 60. Everybody enjoyed the 2-hour lecture by Capt. Tsukahara and Mr. Nakagawa. The Q&A session after the lecture did not come to an end even when one hour had already elapsed (the scheduled time length for the Q&A session was 30 minutes).

Toshiyuki Inagaki, Chair

Japan Chapter

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REL/CPMT/ED Singapore Chapter

-by Dr. Kin Leong Pey

1. Technical Talks

The Chapter organized the following Reliability-related technical talks during August-October 2004:

· Aug 04, Dr **Ahila Krishnamoorthy,** Institute of Microelectronics, Singapore gave a talk on "Interfacial engineering to improve the reliability of Cu interconnects".

· Oct 11, Dr. Professor Arun N. Chandorkar of Indian Institute of Technology, Bombay, India gave a talk on "Technology scaling and its influence on architecture designs".

These technical talks were well attended by members, professionals and students.

2. Technical Seminars

Two IEDM video short courses were arranged in Sep'04. Due to an overwhelming response, three separate viewing sessions were conducted for one of the courses.

· Sep 19 & 24 and 2 Oct, Course 1 - The Future of Semiconductor Manufacturing

· Sep 22, Course 2 - Silicon +: Augmented Silicon Technology

3. Course

A one-day short course on "Integration of Copper with Low-k Dielectrics" by Dr Jeffrey Gambino, IBM, USA was held on 25 October 2004 at the Sheraton Towers, Singapore.

4. Conference

The 2005 International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA'05), organized by the IEEE Rel/CPMT/ED Singapore Chapter, and technically co-sponsored by the IEEE EDS and Reliability will be held at Shahgri-La's Rasa Sentosa Resort, Singapore, 27 – 31 June 2005. The second for papers has been announced. For more information, please visit the IPFA'05 website at http://www.ewh.ieee.org/reg/10/ipfa/html/2005/.

5. Others

The Chapter donated S$500 to the Student Chapter of the Nanyang Technological University branch for a "Back to the Future" competition for post-graduate students.

6. Plans

A one-day short course on "Failure Mechanisms and Reliability in Integrated Circuits" by Dr. M.K. Radhakrishnan, NanoRel Consultants will be held on 10 December 2004 at the Sheraton Towers Singapore.

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Here is a summary of what the Twin Cities RS is doing.

Sept 21, 2004 Had Erik Borgstrom of Environ speaking on EMC - problems and solutions. 17 people attended.

October 19, 2004 was Bob Schlentz spoke on Human Reliability to 18 people.

Nov. 16, 2004 was Eric Ware of Guidant speaking on Distributional Analysis of Biomedical equipment to 15 people.

The January Meeting is planned for Kevin Becker of Hutchinson Technology speaking on Ultrasonic Accelerated Testing Disk Drive Suspension Assemblies on Jan 18, 2005.

Jim McLinn
Twin Cities RS Treasurer

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CPMT (CPM T21) & Reliability Chapter (R07) Report to Committee for 20th Oct 2004

by Nihal Sinnadurai

Chapter: Reliability & CPMT - in existence for 2 years

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Chapter Committee:

• Chairman

• Secretary: (Tony Corless)

• RI representative: Dr John Barrett

• Region Member: David Whalley

• Member Dr Daya Ranasinghe - Nokia.

Events

1. MicroTech 2004, Conference + Tabletop Exhibition

co-sponsored with IMAPS-UK, 3-4 March 2004, Moller Centre, Cambridge

Topics: Medical Electronics, Photonics, Market Watch

Outcome: 16 Exhibitors, 80 Conference Attendees (approx 30 IEEE members)

Finance: IEEE budget = Nil, IEEE expenditure = Nil, IEEE income = nil.

IEEE claimed benefit = 1 event attended by IEEE members.

2. Industry day, Networking + Tabletop Exhibition

co-sponsored with IMAPS-UK, 22 September 2004, Haydon Centre, Swindon

Event objective was to provide a forum for networking between industries involved in electronics between chip and system

Outcome: 10 Exhibitors, 40 industrial attendees, who hailed the event as a success

Finance: IEEE budget = Nil, IEEE expenditure = Nil, IEEE income = nil.

IEEE claimed benefit = 1 event attended by Industry

Next events

MicroTech 2005, Conference + Tabletop Exhibition

co-sponsored with IMAPS-UK, 1-2 March 2005, Moller Centre, Cambridge

Topics: Electronics Packaging, Flip Chip Technologies, Photonics & Power Packaging, Packaging Reliability,

RF Packaging, MEMs Packaging, , Market Watch

Finance: IEEE budget = Nil, IEEE expenditure = Nil, IEEE income = nil.

Proposed Master Classes, jointly with ATTAC, 27-28 February 2005

• Electronics Reliability

• Photonics Reliability

• Introduction to Microelectronics Packaging

Master Class

- **Electronics Reliability Methodology**
- **Photonics Reliability Assurance**

2 half-day Intensive Tutorials

28th February 2005

Møller Conference Centre - Cambridge UK

For more information – Master Class Brochure

CAD, Concurrent Engineering, and Expert Systems

Dennis Hoffman , Committee member

Keith Janasak , Chair of theCAD, Concurrent Engineering, and Expert Systems

Reliability and Maintainability (R&M)Computer-Aided-Engineering (CAE)

R&M CAE applications continue to evolve each year. Refinements are being made but there really hasn't been revolutionary new products. Multiple user environments and multiple user access over the web have added a lot of usefulness and flexibility to the user community. Collaborative enablers such as Net Meeting type applications have really helped with multiple site communications. Data interchange within a discipline as well as between disciplines has become easier.

Probabilistic Technology (PT) as applied to R&M CAE is perhaps the primary focus of next generation R&M CAE tools. Essentially these types of tools allow the user to incorporate parameter variability into their analyses. The US Army Armament Research, Development & Engineering Center (ARDEC) is championing the incorporation of probabilistic methods into an integrated R&M CAE tool environment. They are leading a team of several tool developers and information integration providers to develop a generic proof of concept R&M Tool Integration Framework that incorporates some PT capabilities. At this point in time, this approach holds promise for platform level R&M analyses, but it is yet to be extended to the subsystem or lower levels. It is however, a significant step forward in that it incorporates PT in R&M tools from a variety of different tool developers and these tools are being integrated into a common framework. The hope is that the generic framework can be somewhat plug and play to allow similar tools from other tool providers to be quickly and cost effectively integrated.

The RAMS Symposium has continued to provide an R&M CAE track including multiple sessions dedicated to R&M CAE. These RAMS R&M CAE sessions allow CAE Suppliers to show their new applications to a broad user community. These sessions also provide a forum for using industry to highlight internally developed applications that were developed because CAE Suppliers did not offer such a product or the Supplier application wasn't adaptable to their needs. These RAMS sessions also provide academics a place to highlight their research and resulting applications. Other related R&M CAE sessions include a R&M Software Application technical session and a Panel presentation on R&M CAE Lessons Learned: Successes and Failures. This type of interaction between the tool providers and the tool users helps provide the CAE Supplier insight into industry needs as well as to application that industry is willing to spend funds.

Prognostics and Health Management (PHM) & Condition Based Maintenance (CBM)

Listed below are a few of the Prognostics and Health Management (PHM) organizations involved in PHM and in developing capabilities and tools to aid in PHM implementation. This is basically the result of a data search, so this data is provided for information only and is only a small snapshot of available data.

Goodrich Fuel & Utility Systems: Products Health and Usage Management Systems (HUMS) for Helicopters (http://www.fus.goodrich.com) – The Goodrich Health and Usage Management System is an IMD-HUMS (Integrated Mechanical Diagnostics-HUMS) assessment system which reduces operation and support (O&S) cost. It automatically tracks usage and limit parameters, calculates flight regime spectra structural life usage, rotor and track balance adjustments, engine health and performance (including power assurance checks), and assesses drive-train component condition. The system supports industry standard CVFDR's (cockpit voice and flight data) interfaces. The accompanying Ground Station Support Package is a self contained Condition Based Maintenance Information Management System. By continuous evaluation of component usage and condition, it can support changing the current method of inspecting and automatically replacing parts solely as a function of flight hours. The current Open architecture system is based upon functional and performance requirements established by the Navy for the H-60, H-53, and by Sikorsky Aircraft Corporation for commercial S-76 and S-92. The current system has been influenced by 10 years of development testing with the Navy, plus the experience gained with earlier HUMS models certified by the Federal Aviation Administration for operation on the Agusta A109K2 and several models of the Eurocopter AS350/355. On-board System Functions -- The on-board system automatically monitors and records data, and executes diagnostics without pilot involvement, and saves data for later analysis on the ground station. Functions include:

- Limit and exceedance monitoring

- Engine performance monitoring

- Automatic cycle counting

- Propulsion system, drivetrain and airframe usage monitoring

- Power assurance

- Regime recognition and time in regime

- Drive-train condition assessment

- Rotor track and balance

Impact Technologies LLC (web site: http://www.impact-tek.com/) is a high-tech engineering consulting and health management system development firm that is dedicated to supplying advanced machinery diagnostic and prognostic solutions and software tools in the aircraft, land-based equipment, power, nuclear and defense industries. Impact possesses a strong vision of the value and future of machinery diagnostics and prognostics, assists customers in the development of customized applications, and produces metrics that justify investment in the technology. New products and services offered:

- GearLife(tm) -- A generic gear prognostic module that integrates the advanced physics-based failure mode modeling, HUMS vibration feature analysis and inspection / operational data to enable gear failure predictions in critical drive train applications.

- Hydraulic Pump Life Monitor(tm) -- State-of-the-art pump health monitoring system.

- ImpactEnergy(tm) -- High frequency vibration diagnostic technique specifically designed for the early detection of bearing failure modes such as spalling, pitting and corrosion.

- Metrics for Diagnostic Technique Qualification & Validation -- The CBM Metrics Test Bench provides a virtual environment for evaluating diagnostic systems on specific machinery applications.

- PHM Design(tm) -- An innovative software tool specifically focused on designing, developing, evaluating and deploying Prognostic and Health Management (PHM) or Condition-Based Maintenance (CBM) systems.

- Smart Oil Sensor (SOS(tm)) -- An Inexpensive, intelligent, and compact fluid management system that features embedded on-line / in-line sensing and on-board processing.

- SensorCheck(tm) -- A plug-in sensor validation module that can be easily customized and applied to any set of critical measurements being monitored in your application. This software integrates advanced signal processing routines with data-driven analysis models to provide an unprecedented level of reliability for measured system parameters.

Prognostic and Health Management Applications:

- PHM Design -- The Prognostics and Health Management (PHM) system design tool integrates a model-based FMECA methodology with state-of-the-art PHM system strategies directly linked to downstream Life Cycle Costs (LCC).

- CBM Metrics Test Bench -- The CBM Metrics Test Bench is a web-based application that provides a virtual laboratory for impartially evaluating the performance and effectiveness of enabling technologies for condition-based maintenance (CBM).

- ADEPT (Aircraft Diagnostic and Engine Prognostic Technologies) – ADEPT is an innovative diagnostic, prognostic and maintenance reasoning web-based application developed in cooperation with the U.S. Army Aviation Technology Directorate and Honeywell Engines whose goal is to significantly reduce operational and support requirements of the T55 engine in the CH-47 (Chinook) helicopter.

Georgia Tech, Intelligent Control Systems Laboratory, Diagnostics And Prognostics, (web site: *http://icsl.marc.gatech.edu/research_and_publications.asp?page=research_and_publications& filename=Diagnostics_and_Prognostics)*. Georgia Tech has an active R&D program in Condition Based Maintenance and Condition Based Logistics dating back to the early 1980s. Researchers in the College of Engineering and the Georgia Tech Research Institute have been conducting research in integrated diagnostics, prognostics and logistics support under sponsorship from government agencies and private industry.

Fault Diagnostics / Prognostics For Equipment Reliability and Health Management *(http://icsl.marc.gatech.edu /03_Fault_Diagnostics2.pdf)* – An intensive four-day course was offered in November 2003 by the faculty and staff of the School of Electrical and Computer Engineering of the Georgia Institute of Technology in collaboration with The Georgia Tech Research Institute, the General Electric Company, Honeywell International and Impact Technologies. The course was to introduce practitioners and researchers in the reliability area to novel concepts and methodologies for machine condition-based maintenance that have been shown to perform reliably and robustly in actual dynamic systems. The industrial and military communities are concerned about critical system / component reliability and availability. They are seeking to maximize equipment uptime while minimizing costs.

This course focused upon an integrated hardware / software approach to machine health maintenance by introducing a systematic framework to failure mode and effects criticality analysis, database management and means to diagnose machine / component impending failure conditions and to prognose their remaining useful lifetime.

U. S. Army Prognostics Framework Research and Development Study, Prognostics Mechanisms Survey Results, Major R&D Efforts:

- Turbine Engines: PNNL; ARL (D)

- Helicopter gearbox prognostics: Princeton and Boeing / Office of Naval Research (ONR) (E)

- CBM for Intelligent Ship: Penn State / ONR (D)

- Obstacle avoidance: Univ. Southampton & UK Dept. of Defense (R/E)

- Power plants Intelligent Data Acquisition & CBM: PAC & PROSIG (U)

- Wind tunnel compressors automated reasoning expert system: AMES Research Center (D)

- Power transmission systems (MURI IPD): Penn State / ONR (R)

- Statistical Network Modeling (ModelQuest): AbTech / Rome Labs (U)

Giordano Automation Corp (http://www.giordano.com/index.htm) is a company whose main focus is the development and application of advanced reasoning technologies to support operations monitoring and efficient maintenance. Their software products encompass the development and execution of operational anomaly analysis and fault diagnostics for complex systems and processes. They believe their technology is at least five years ahead of the state-of-the-art. The goal in their web site is to introduce you to commercial, off-the-shelf products and application services, and to show you how their innovative technology can solve your operations and maintenance needs. Products:

- Diagnostic Profiler

- Diagnostician

- Prognostics Framework

- Operator Debrief

- Adaptive Training

- Diagnostic Workbench

- Class V Services

Pennsylvania State University, The Applied Research Laboratory, Systems and Operations Automation Division *(web site: http://www.arl.psu.edu/capabilities/ins_soa.html)* -- The Systems and Operations Automation (SOA) Division of the Penn State Applied Research Laboratory was formed to address the emerging fields of condition-based maintenance (CBM) and advanced sensing and control. The division provides valuable research and development efforts in these areas to support the U.S. Department of Defense and U.S. industry.

Oceana Sensor, Wireless e-Diagnostics

(web site: *http://www.oceanasensor.com/Company/profile.htm)* -- In The Blink Of An Eye, Missions Often Fail. We Never Blink. Wouldn't it be valuable to see problems before they occur? To know when a piece of equipment or machinery in your system is going to fail before it actually happens. Imagine how much you'd save in dollars, time and manpower. This strategic vision is available from Oceana Sensor, a manufacturer of sensing systems for a wide variety of applications including machinery health monitoring. All types of industries and measurement services use their sensors and data collection tools to monitor mission-critical operations and assess when components need replacement or repair. Drawing on more than 30 years of experience in sensor manufacturing, Oceana Sensors have the skill to provide a sensing tool for virtually any need.

Spray Cooling Technology

ISR (Web site: *http://www.spraycool.com/main2.htm)* -- Many challenges are created in the drive toward developing and deploying higher performance low cost electronic systems. Packaging densities are increasing, while at the same time individual components draw more power, creating the need for high performance cooling. Cooling is not the only obstacle. High performance electronics must be deployed in different operating environments ranging from data centers to the factory floor, outdoor environments, even in the battlefield. ISR's Spray-cooling techniques and their associated chassis solve these problems. Using custom, closed-loop liquid-cooled systems, leading-edge commercial convection cooled modules can be deployed in the harshest of military

environments without the disadvantages of other approaches.

Lead Free and Green Electronics

University Of Maryland, CALCE Electronic Products and Systems Center

(web site: *http://www.calce.umd.edu*) -- CALCE's Lead Free Forum is dedicated to the collection, generation, organization, and dissemination of information related in the manufacture, assembly, and fielding of lead free and "green" electronic products and systems. Current issues and events:

- Lead-free Electronic - 2004 Edition A new reference book for Pb-free electronics is now available from CALCE EPRC Press.

- CALCE Pb-Free Patent Finder Software (CALCE Consortium Members' Only) -- A software tool for examining existing international patents for Pb-Free Solders. (Updated Version 1.0.1 posted 2/17/04)

- Tin Whisker Studies Information related to the tin whisker as a potential source of failure in electronic hardware.

- Failures in Microeletronics Attributed to Phosphorus -- An update to the warning of a potential reliability risks attributed to molding compounds that use phosphorus as a flame-retardant.

CALCE Tin Whisker Alert: A failure mode is re-emerging that has been responsible for the loss of billions of dollars worth of satellites, missiles and other equipment - electrically conductive 'tin whiskers'. Tin whiskers can develop under typical operating conditions on any product type that uses lead-free pure tin coatings. Driven by the accelerating movement to lead-free products, tin whiskers pose major safety, reliability and potential liability threats to all makers and users of high reliability electronics and associated hardware. Existing approaches are not sufficient to control tin whiskering in high-reliability systems. The risk is here now, and unless decisive action is taken soon to fund development and implementation of a strategic action plan to devise short-term stopgap procedures and medium-term investigation of mitigation alternatives, serious consequences

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Mechanical Reliability

Richard L. Doyle P.E.

Chair of Mechanical Reliability

Mechanical reliability engineering is becoming increasingly important, particularly as it relates to the development of Microelectornics and Nano-Devices. Both Microelectromechanical Systems (MEMS) and Nanoelectromechanical Systems (NEMS) are being investigated for diverse applications. These new technologies require high reliability, while just the opposite may result. It is important that these new products provide the desired or expected reliability. This makes it necessity to predict the failure rates and implement Reliability by Design for this new technology.

The purpose of a Reliability analysis for Microelectromechanical and Nano-devices is to provide a realistic estimate of the reliability of extremely small parts or structures. This estimate may be used as a basis for reliability improvements through design changes or to predict if the desired reliability of the system has been achieved. It is difficult to establish a good estimate of reliability without an organized and proper approach. This requires all of the techniques available in classical reliability analysis including: determining the strength of the materials, determining the loads, performing a mechanical stress analysis, determining the failure modes, and recommending design changes.

As the analysis progresses, one should reevaluate reliability goals and modify the design of the Micro or Nano device to ensure that these goals are met. If the product cannot be modified, then the prediction provides the best estimate of the expected life and reliability of the device.

These MEMS and NEMS devices include: electronic devices, sensors, magnetic devices and mechanical devices.

The Predicted Reliability values shall be calculated for all major components in the system. The individual part failure rate is determined using classical mechanical reliability predictions. If test results are available, this provides the best reliability estimate and a mechanical stress analysis will provide appropriate parametric tradeoffs. The component reliability values are combined using series or parallel redundancy depending on the design. This will provide the Predicted Reliability values for the MEMS and NEMS devices and Mechanical system.

Environmental conditions become critical for the MEMS and NEMS devices. This includes such influences as moisture, temperature, thermal stresses, mechanical shock and vibration. For vibration, it may be necessary to provide a mechanical support, including trenches for wires, etc. Vibration and shock may be the highest loads. If mechanical failures occur, changing the design may be a solution or it may be necessary to obtain different materials.

Most reliability computer programs have a form of mechanical reliability analysis that will provide tradeoffs in the parameters listed in the preceding paragraphs. The program will also provide a prediction of the failure rate of the device or part. These programs along with mechanical stress analysis programs allow for a controlled analysis for parametric studies and correlation with actual test results.

These miniature devices will be found in a growing number of applications. Some present applications include:

A. Computers: Next generation high speed computers.

B. Space Applications: High efficiency, high bandwidth electronic devices for: Telecommunications and Television transmission, Weather measurement, determining Ocean and Atmospheric conditions, and sensors for deep space.

C. Automotive Industry: High strength, light weight sensors.

These are just a few of the industries requiring high reliability in their Micro and Nano mechanical products.

Microelectronics Reliability

Alan Street

Chair of Microelectronics Reliability

With new materials being introduced into mainstream IC processes, new reliability problems are emerging. At the transistor level silicon dioxide is beginning to be replaced by higher-K materials, while copper metallization and low-K dielectrics are now in common use in the “back end of line” (BEOL) processes. The following two articles appeared in EE Times, and highlight some of the reliability issues facing IC manufacturers today. The source for this material was Reliability Society sponsored International Reliability Physics Symposium (IRPS).

DALLAS — With the difficult integration of copper largely complete and the onerous effort to bring low-k dielectrics to the interconnect stack well under way, technologists are moving to what could be an even more challenging task: replacing silicon dioxide with high-k dielectrics as the gate insulator.

High-k materials such as hafnium oxide and zirconium oxide exhibit a tendency to "trap" electrons. At the International Reliability Physics Symposium here last week, technologists engaged in a furious debate over whether mobility degradation and threshold voltage instability are problems intrinsic to all metallic high-k materials.

Regardless of whether they deemed high-k's problems intrinsic, many of the researchers attending IRPS predicted that the high-k introduction will prove far more nettlesome than either the copper or the low-k transitions. "SiO2 is at the very heart of the transistor, and replacing it is like performing a heart transplant," said Robin Degraeve, a researcher at the Interuniversity Microelectronics Center (IMEC) based in Leuven, Belgium.

Nevertheless, the industry is prepping for the surgery.

Mark Bohr, director of process architecture and development at Intel Corp., said Intel has "zeroed in on a high-k material. I won't say what that material is just yet, but one thing is for sure: It is not a simple drop-in."

Intel is nonetheless optimistic, Bohr said, that with better control of the deposition of high-k materials, charge trapping in the interface layers between the high-k material and the silicon channel can be improved.

"We don't think the charge-trapping problem is principally in the high-k material itself. Most of the charge is being trapped in the interface layers," Bohr said after his keynote at IRPS. "But improving those interfaces presents formidable challenges," he acknowledged.

As current leakage at the gate worsens, most technologists say, high-k materials will be needed to control power consumption in both low-power and high-performance chips. While the brute scaling of silicon dioxide has gone better than many in the industry expected, electrons increasingly are able to burrow through the progressively thinner silicon dioxide layer, sending leakage current skyrocketing.

As Intel's microprocessors move to billion-transistor densities by 2007, controlling power could mandate the use of high-k materials as soon as the 65-nm node, Bohr said. "If we have a high-k material by then that works, we will use it," he said.

Hafnium oxide, zirconium oxide and high-k materials have an intrinsic tendency to trap electrons, said Glenn Alers, a physicist working at Novellus Systems Inc. (San Jose, Calif.). "The metal atoms in these high-k materials do not all bond well, leaving dangling pairs. And as the k-value increases, the bandgap of the dielectric decreases, and electrons can penetrate into the dielectric more easily. Those intrinsic properties make it much more likely for defects and traps to form" in the high-k materials than in SiO2, Alers said.

Ashraf Alam, a gate oxide research manager at Agere Systems (Allentown, Pa.), said that in order to limit voids between the insulator and the silicon channel, the high-k layer often is grown on top of an interfacial layer of silicon dioxide of 4 to 10 angstroms.

"The high-k layer must be relatively thick, in the range of 3 to 4 nanometers 30 to 40 angstroms, so that the high-k molecules can cross-link with neighboring atoms," Alam said. "Those molecules are relatively rich in electrons compared with silicon dioxide, thus the higher rates of charge trapping."

IMEC's Degraeve said the center's researchers have reached some disturbing early conclusions about the high-k transition. When voltages are applied to test circuits, he said, high-k materials exhibit "significant and immediate shifts in threshold voltage" that are attributable to charge trapping.

Some believe this threshold voltage instability may be predictable, with design-around solutions. But Degraeve said the shifts are so large-measuring as high as 80 to 100 millivolts under the pulsed conditions typical during IC operation-there is no clear way to design around them.

For an IC operating at 1 V, with a threshold voltage of 400 mV or so, a shift of 80 to 100 mV in the threshold voltage would present enormous challenges to circuit designers. The shifts would make analog circuit design, which is sensitive to very small changes in threshold voltage, particularly challenging.

"This is an intrinsic property of high-k materials, and there are no indications about how to solve these issues," Degraeve said. The question for designers is, Can you live with it?"

Voltage instability is "very difficult to get rid of," he said. "The charge-trapping effect is extremely fast and immediately reversible." That is, when a voltage is no longer applied, the trapped electrons flow out of the insulator. SiO_2, by contrast, builds up trapped charges gradually, over a period of years.

The IMEC team has tested many combinations of high-k insulators, Degraeve said, and all exhibit charge trapping. The most promising material from a process stability stance is hafnium oxide, he said.

Texas Instruments Inc. reliability engineer Ajit Shanware presented a more encouraging picture. TI, he said, plans to use a hafnium silicate dielectric with a k-value of 13, a so-called medium-k material that bridges between silicon dioxide and the higher-k metallic oxides.

At IRPS, Shanware said the HfSiN material causes threshold voltage instability of about 10 mV-far lower than the 80 to 100mV IMEC warned of-in NMOS transistors. "We believe the threshold voltage instability is mainly due to stress, rather than electron trapping, and that most of the charge trapping is near the interface" with the silicon channel, he said.

With more careful control of the stressed interface between the channel and the high-k oxide layer, further improvements can be expected, Shanware said. But he acknowledged it will take time to work out the myriad process issues.

Luigi Colombo, who heads TI's high-k oxide development group, said that his company knew of "no conclusive experimental or theoretical evidence that high-k instability is a fundamental problem" and insisted, "With control of defects, and proper materials selection, the industry should be able to overcome its current limitations."

But others warned that voltage instability and mobility degradation can be more pronounced in PMOS transistors than in the NMOS devices TI discussed.

Max Fischetti, an electron transport physicist at IBM's Thomas J. Watson Research Center (Yorktown Heights, N.Y.), said he believes high-k materials have intrinsic mobility degradation properties but that process control improvements might at least contain the degree of mobility degradation to the intrinsic level. The problem is that the industry doesn't have much time.

While MOSFETs were proposed in the late 1930s, it wasn't until 1964 that the industry's pioneers, including Intel's Andrew Grove, realized circuit instabilities were caused by potassium and sodium contamination in the SiO_2, Fischetti said. Since that breakthrough, "we've had three decades to study silicon dioxide-but the industry wants to bring in high-k materials very quickly, in this decade."

Asked in an interview to reconcile the differences between the IMEC and TI presentations, Fischetti said, "I'm not surprised that these labs are reporting inconsistent results. While we are all learning fast, these processes are not very well-controlled yet. The annealing steps, the deposition and growth techniques, all require a lot more optimization-but we don't have much time before these new materials may be needed."

The industry has seen "pretty promising results" from silicates, such as zirconium silicate and hafnium silicate, he said, but "when we try to measure the mobility, for most transistors with these high-k materials it is pretty bad." Degradation ranges "from 30 percent up to a factor of two compared with the universal mobility curve. A 30 percent hit is not good news."

The hit to mobility is intrinsic, Fischetti said, because as the dielectric constant increases, the electrons tend to polarize, and the bandgap decreases sharply. The phonons in high-k materials vibrate with a frequency that results in softer atomic bonds, which lead to charge trapping.

"There are dark areas in the theory, and at the experimental level we don't know exactly where we are with some deposition techniques," Fischetti said. "So I take some of these early results with a grain of salt. But if the problems are intrinsic because of remote scattering of the optical phonons-if that is true-then we could be in bad shape."

Austin, Texas - After perhaps a year of trashed schedules caused by problems with interconnect vias and with packaging, several companies are starting volume shipments of chips with low-k dielectrics. Agere Systems, LSI Logic, Motorola, TSMC and Texas Instruments each say they are ready to produce low-k-enabled 130-nanometer products. IBM Corp. is shipping some product with low-k dielectrics in flip-chip packages, and United

Microelectronics Corp. says it will bring low-k 90-nm products to market late this year.

These porous materials-with a k-value of less than 3-have caused major headaches. Thermal expansion of the low-k material caused vias to pop off copper wires, as the low-k insulation expanded faster than the wires did. Then came packaging challenges: The low-k materials were so soft that it was difficult to attach a die to a package without damaging the chip.

Indeed, the move from fluorine-doped silicon dioxide to low-k dielectrics "opened up a Pandora's box of new failure modes," said Ted Dellin, a researcher at the Sandia National Laboratories. "Low-k is a sober reminder of just how difficult it is to introduce a new material," Dellin said at the recent International Reliability Physics Symposium (IRPS) in Dallas.

Agere Systems Inc. early this month claimed to be the first supplier to launch volume shipments of a low-k product: a communications IC produced in the low-k process of Taiwan Semiconductor Manufacturing Co. Agere is aiming the DSP-16411 at cellular basestations. Steve Hillenius, director of device technology, said the DSP was made "10 to 15 percent faster by using low-k" compared with its predecessor, the three-year-old DSP16410. Agere's 411 DSP is shipping in a 208-pin plastic BGA.

Shang-yi Chiang, a senior vice president in charge of the R&D group at TSMC, said the foundry has a handful of chip customers qualified at 130-nm design rules and ready to launch products that take advantage of the faster interconnects that low-k insulators support. TSMC some months ago resolved a set of low-k-related stress-migration issues that affected vias, he said, and then turned to packaging challenges such as development of underfill and molding compounds that could alleviate stress on the die inside a package. "The industry really underestimated the difficulties with low-k," Chiang said at IRPS.

LSI Logic Corp. said in late March that it is production-ready with flip-chip packages for dice made at TSMC on a process that uses the Black Diamond low-k dielectric, a chemical vapor deposition (CVD) material from Applied Materials Inc. with a k-value of 2.9. Stan Mihelcic, senior manager of advanced packaging solutions at LSI Logic, said the porous nature of low-k materials demands special care to ensure that the stresses placed on a die within a package do not cause interconnect delamination.

High I/O count

LSI Logic offers three plastic flip-chip BGAs, starting with low-cost substrates that place solder bumps on the periphery of a die. The high-end package supports signal I/O placement in the core region of a die. Because the I/O slots can be placed toward the center of a die, smaller die sizes with as many as 1,750 I/O signals are possible, Mihelcic said. Amkor Corp. has licensed the flip-chip process for low-k dice and is reportedly ready for volume production.

Motorola Inc. applied low-k materials to a PowerPC processor made with 0.18-micron design rules, said Dirk Wristers, director of device integration at the MOS-13 fabrication facility here. "We've ob-served a 20 percent frequency improvement, and a 3 to 5 percent improvement in power, with no degradation in yield."

Motorola replaced a fluorinated oxide with a k-value of 3.6 with the Black Diamond material for this version of the PowerPC and is in the process of bringing out several 0.13-micron parts that also use low-k dielectrics, Wristers said.

Texas Instruments Inc. is qualifying an Ultrasparc processor made for Sun Microsystems Inc. that uses Corel, a carbon-doped oxide material from Novellus Systems that is applied with CVD equipment. TI said it will use Corel throughout its 90-nm process as it moves into volume production at the end of this year.

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2005 International Conference on Asian Green Electronics - Design for Manufacturability and Reliability (2005AGEC). The conference will be held on March 15-18. The purpose of the conference is to present the latest advancements in environmentally compatible electronics design, manufacturing and packaging technology. The goal is to help electronics companies' design and manufacture green electronics products for the global market.

The conference will cover the following topics:

- Design for green electronics
- Green manufacturing technologies including lead-free solders, conductive adhesives and other green technologies
- Halogen free substrates
- Environmentally Friendly Packaging and Design Technologies
- Life Cycle Analysis and Assessment
- Life Cycle Cost Analysis
- Life Cycle Data Management

You are welcome to visit the website of the conference we have organized in Shenzhen last January for your reference > http://www.ee.cityu.edu.hk/~agec/ . It would be nice if your could let me know the possiblity at an early date.

2005 AGEC BROCHURE

Angie Wong

Conference Secretary

EPA Centre, City University of Hong Kong

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CALL FOR ABSTRACTS

Second International Workshop on Nano & Bio-Electronic Packaging
March 22-23, 2005, Atlanta, Georgia
Georgia Tech's Technology Square Research Building

Program Agenda and Further Information: www.prc.gatech.edu/nanobiopack
Download event flyer (PDF)

The "Second International Workshop on Nano and Bio-electronics Packaging" is a two-day event offering informative keynote presentations and technical sessions on Nano technology. The currently scheduled technical sessions and their chairs are as follows:

Nano Package Design
James Libous - IBM & Madhavan Swaminathan - Georgia Tech

Nano Biomedical Packaging
Jorma Kivilathi - Helsinki University of Technology and Terry Dishongh - Intel

Nano Photonics
Avi Bar-Cohen - University of Maryland and Ephraim Suhir - Designed Nano-Materials

Nano Packaging Materials
Goran Matijasevic - University of California

Nano Manufacturing
Srinivas Rao - Solectron and Randy Rannow - Hewlett-Packard

Industry Perspective
Charles Lee - Infineon, Singapore

NEMS & Fluidics
Michael Wahl - University of Siegen

Nano Interconnections
Andrew Tay, National University of Singapore

Nano Lithography
Ajay Malshe, University of Arkansas

Nano Testing, Modeling and Imaging
Sheng Liu, Wayne State University

Conference Coordinator: Dr. Swapan Bhattacharya (swapan@ee.gatech.edu)

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Dear Colleague:

We would like to bring to your attention that the 2nd Conference on
Nanoscale Devices and System Integration (NDSI) will be held in Houston, Texas on April 4-6, 2005.

NDSI, sponsored by IEEE Nanotechnology Council, is a highly interactive meeting, serving as an open forum to identify priorities in today's broad range of nanoscale technologies.

The meeting has a single session format with the invited talks forming the body of the conference. Contributed work is showcased at several poster sessions throughout the conference. The quality of the technical program is ensured by the broad participation of the nanotechnology leaders from both industry and academia.

Contributed paper submissions are welcome. The submission instructions and digest format can be found at <http://www.nanointernational.org/call_for_papers.htm.

Major topics related to device fabrication/synthesis at the nanoscale and integration of nanoscale technologies into functional systems will be covered, including:

* Nanoelectronics
* Nanomagnetics and Spintronics
* Nanophotonics
* Nano/bio inspired devices and system
* Nanorobotics
* Materials for Nanotechnologies
* Fabrication for nanoscale devices
* Metrology

Work presented at the conference will be published in a special issue of IEEE Transactions on Nanotechnology, subject to the usual peer-review process.

Houston is beautiful this time of year and the conference hotel is nestled in the museum district overlooking one of Houston's most beautiful parks. Sports venues and recently revitalized downtown Houston are a few minutes away by light rail.

Additional information about the conference can be found at
<http://www.nanointernational.com. If you did not receive this message
directly and would like to receive future NDSI announcements, please send an e-mail to
ndsi@nanointernational.org
<mailto:ndsi@nanointernational.org> and your name will be added to the
mailing list.

Thank you for your attention.

NDSI'05 Organizing Committee

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Call for Papers - International Symposium on Stochastic Models in Reliability, Safety, Security and Logistics (SMRSSL '05)

BROCHURE

Dear Colleague:

I am pleased and honored to invite you to participate in the International Symposium on Stochastic Models in Reliability, Safety, Security and Logistics (SMRSSL '05), to be held on February 15-17, 2005 at the Sami Shamoon College of Engineering (formerly NACE), Beer Sheva, Israel.

This Symposium will constitute a forum for discussing different issues of Stochastic Models in Reliability, Safety, Security and Logistics with respect to their applications. The conference objective is to assemble researchers and practitioners from universities, institutions and industries from around the world, involved in these fields, and to encourage mutual exchange.

Common methods and models will be considered from a general point of view; theoretical modeling, computational and case studies will range from academic considerations to industrial approaches, as well as emphasizing topics on cooperation between industries and research institutions. The cooperation that will contribute to the advancement of research and solutions to engineering issues is of utmost importance.

Within the framework of the conference, research and practical lectures will take place at parallel sessions. Therefore, we will be inviting PhD researchers to submit papers relevant to the topic.

We warmly invite you to share and enjoy with us a stimulating program at the Symposium and sample the historical atmosphere of Beer Sheva and its captivating heritage.

Please, visit our web-site http://www.nace.ac.il/extra/SMRSSL05/

Sincerely,

Dr. Ilia B. Frenkel
Co-Chairman
International Symposium on Stochastic Models in Reliability, Safety, Security and Logistics
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NPL develops new instrument for measuring solder properties

National Physical Laboratory has developed a new instrument for measuring solder properties.

With the take up of the new lead-free alloys there is an imperative to obtain accurate material properties. Today there is a realization that these properties must be measured on volumes of materials typical of current solder joints (under 1mm³).

This requirement is challenging in terms of instrument sensitivity, requiring the ability to measure and displace small distances, typically a few micrometers to a precision of 0.1µm, and to measure low forces. NPL has developed a machine that achieves this capability and is based on a novel configuration.

Measurements are now possible at typical stresses and strains found in solder joints, resulting in realistic fatigue and creep rates to be measured. These values are essential for accurate statistically based life-time predictions of lead-free reliability. This work has been carried out at NPL by Milos Dusek and Crispin Allen.